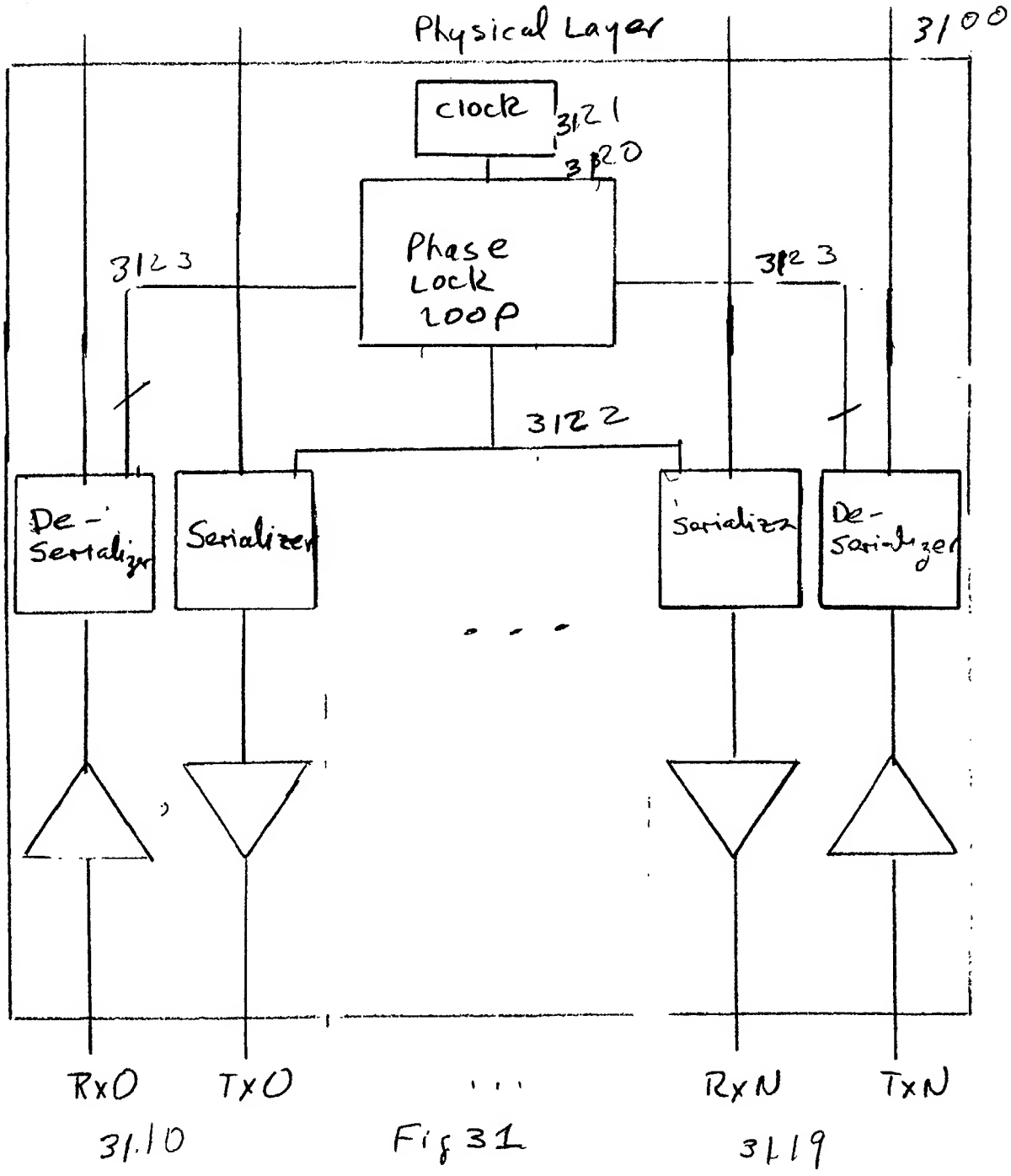



Fig 31

Input Queue 3201

| Port | R/W | Address | Data |
|---|---|---|---|
| 3 | R | 1000 | |
| 4 | W | 4000 | 10....1 |
| 3 | W | 1000 | 111...0 |
| 3 | R | 2000 | |
| | ⋮ | | |

Output Queue 3202

| Valid | Port | Data |
|---|---|---|
| 1 | 3 | 11...0 |
| 0 | | |
| 0 | | |
| 1 | 3 | 101...1 |
| | ⋮ | |

Fig 32

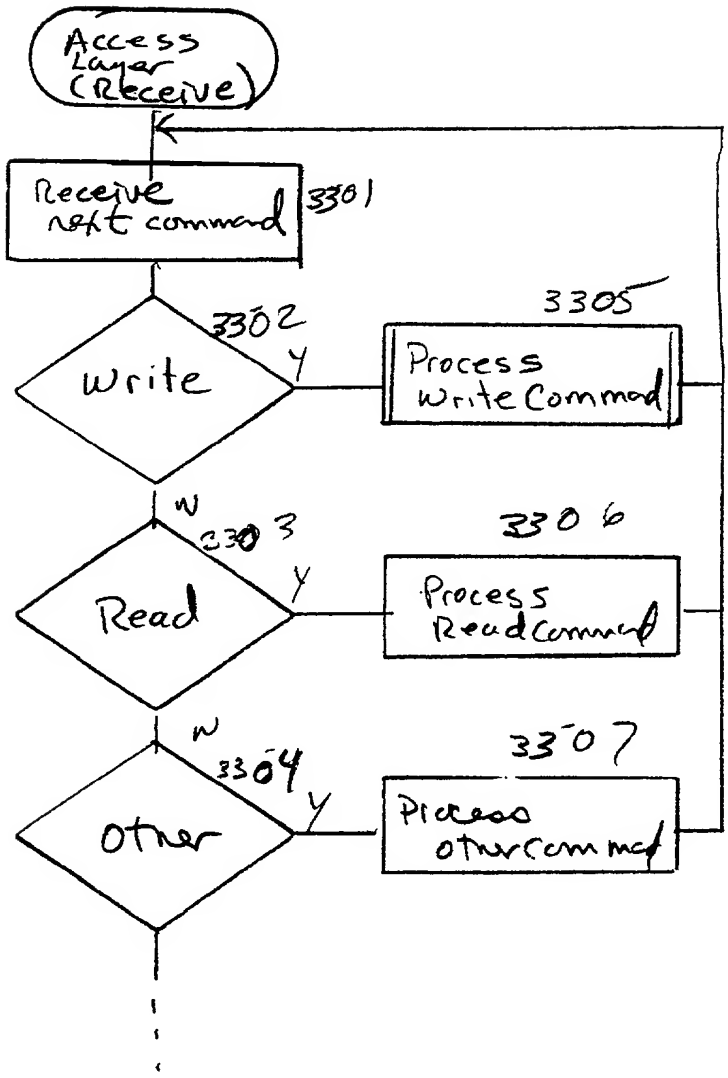

Access Layer (Receive)
Receive next command
3301
Write
3302
Y
Process Write Command
3305
N
Read
3303
Y
Process Read Command
3306
N
Other
3304
Y
Process other command
3307

Fig 33

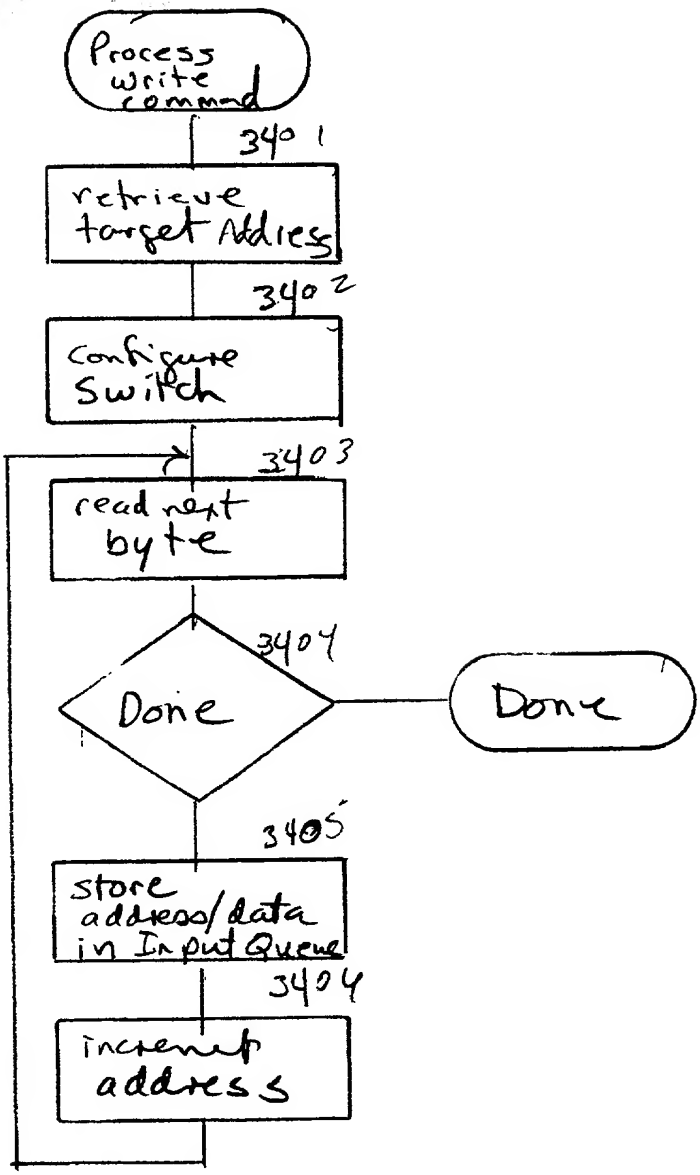

Process write command
3401
retrieve target Address
3402
configure switch
3403
read next byte
3404
Done
Done
3405
store address/data in Input Queue
3404
increment address

Fig 34

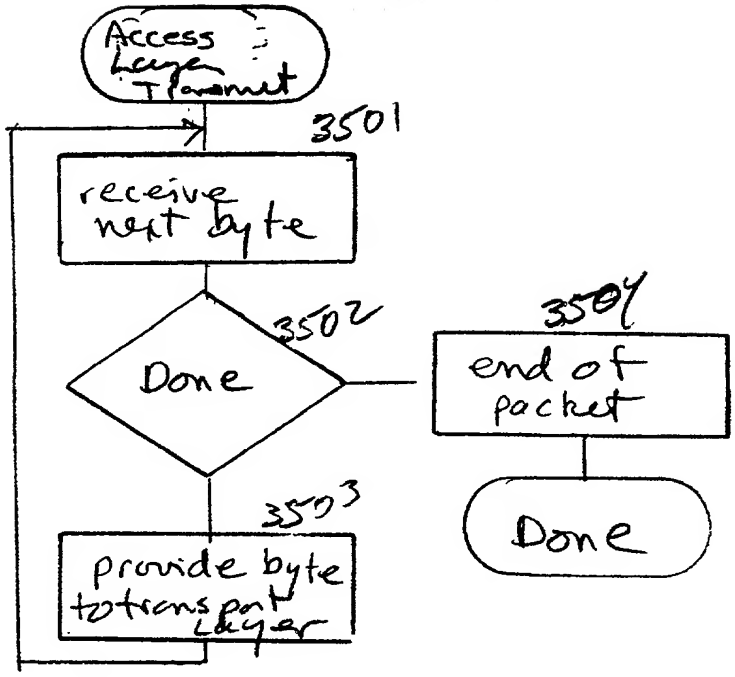

Access Layer Format
3501
receive next byte
3502
Done
3504
end of packet
Done
3503
provide byte to transport Layer

Fig 35

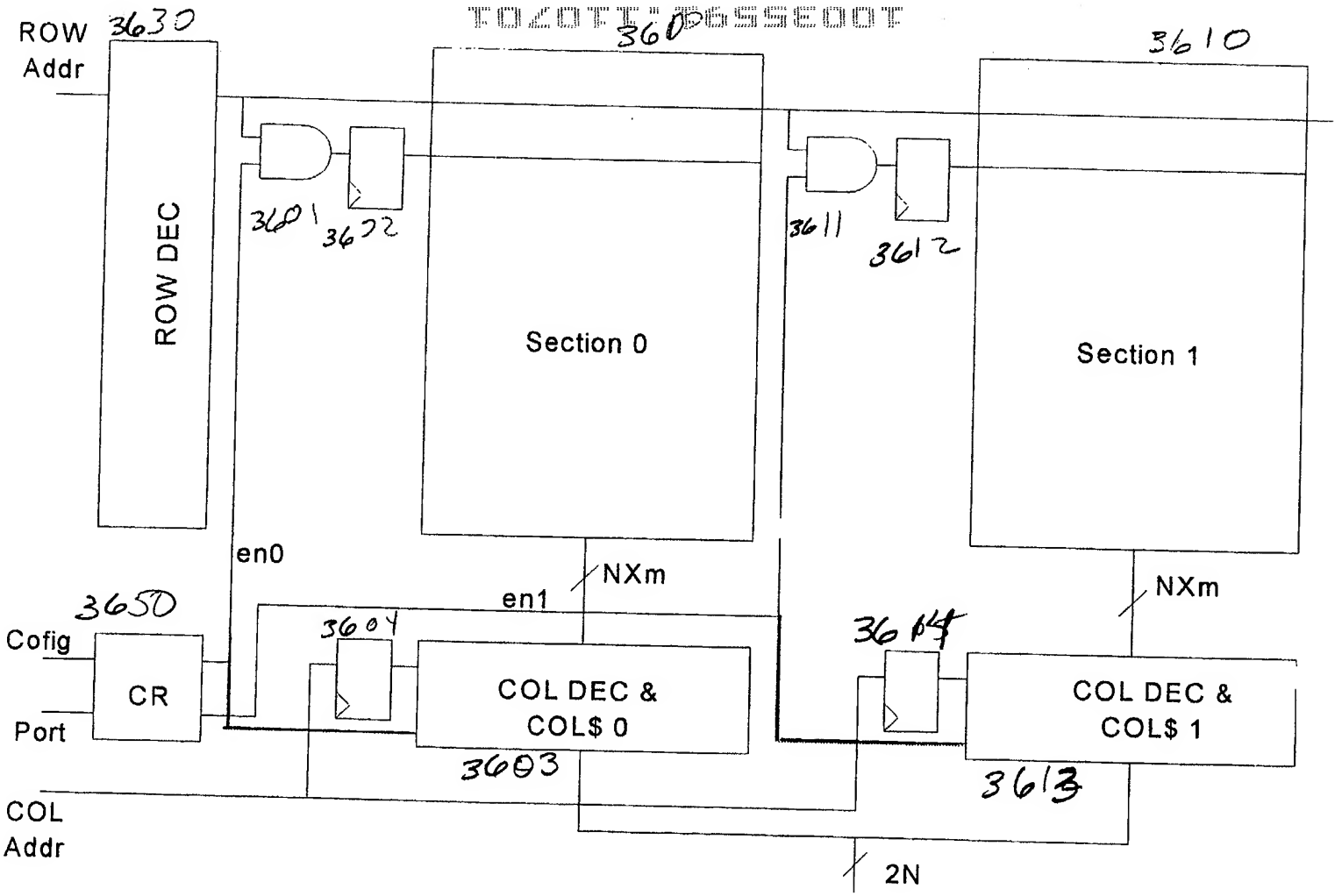
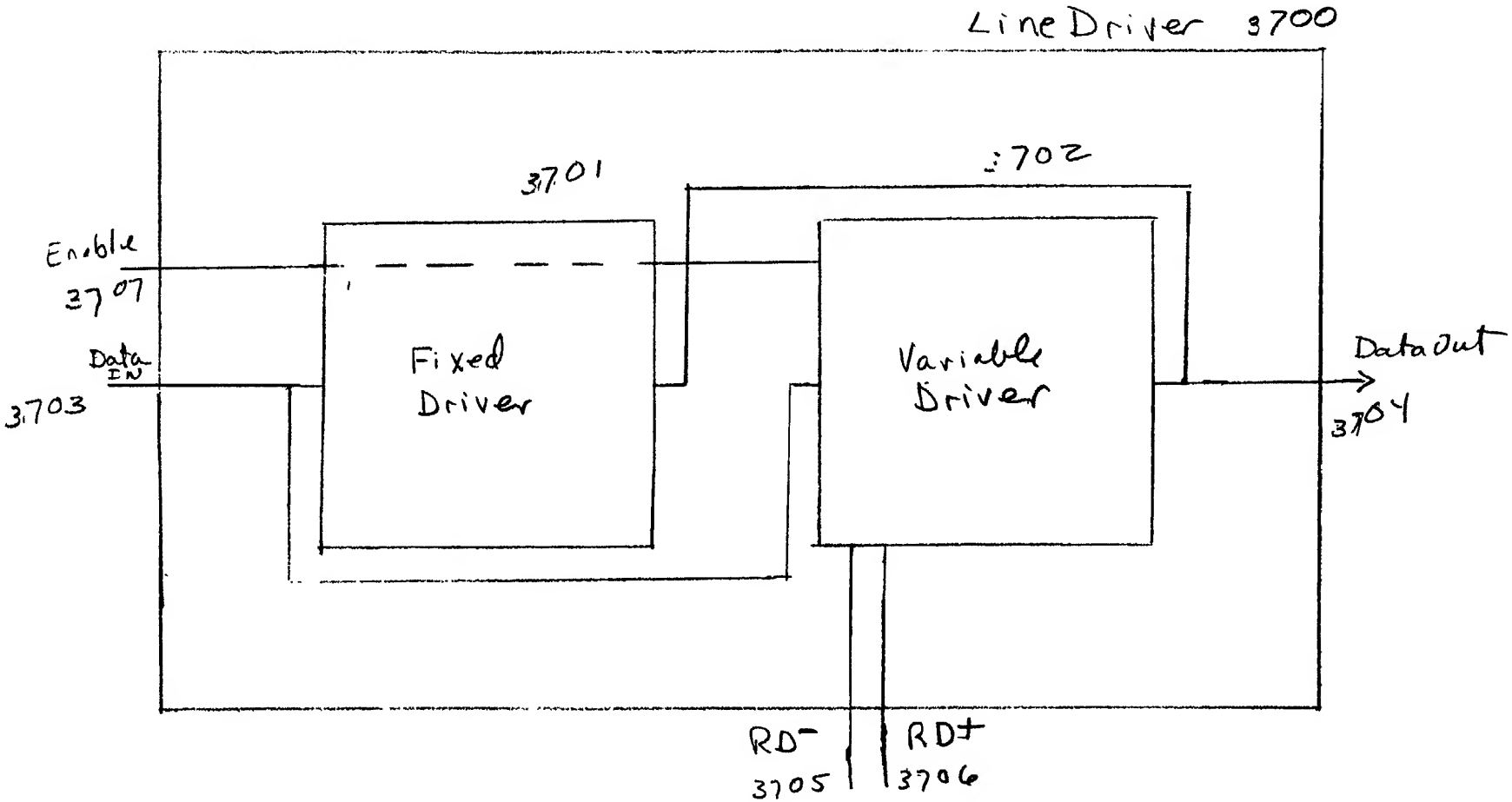

ROW
Addr
3630
ROW DEC
3601
3602
Section 0
3610
3611
3612
Section 1
en0
NXm
en1
NXm
3650
Cofig
Port
CR
3604
COL DEC &
COL$ 0
3603
3614
COL DEC &
COL$ 1
3613
COL
Addr
2N

Fig 36




Variable Driver

$\begin{cases} RD^+ \wedge \overline{DataIN} = \text{pull down} \\ RD^- \wedge DataIN = \text{pull up} \end{cases}$

Fig 37A

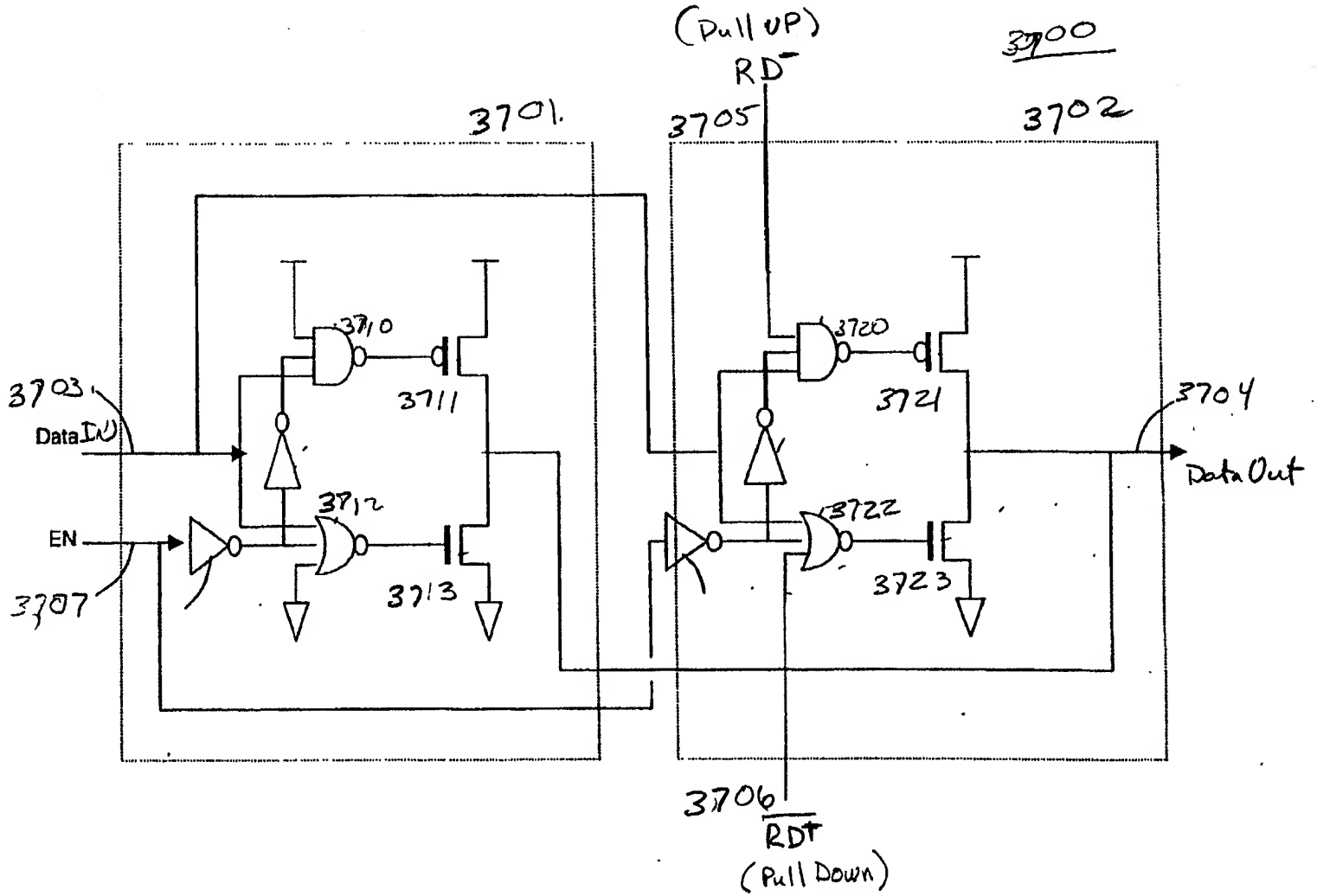



Fig 37B

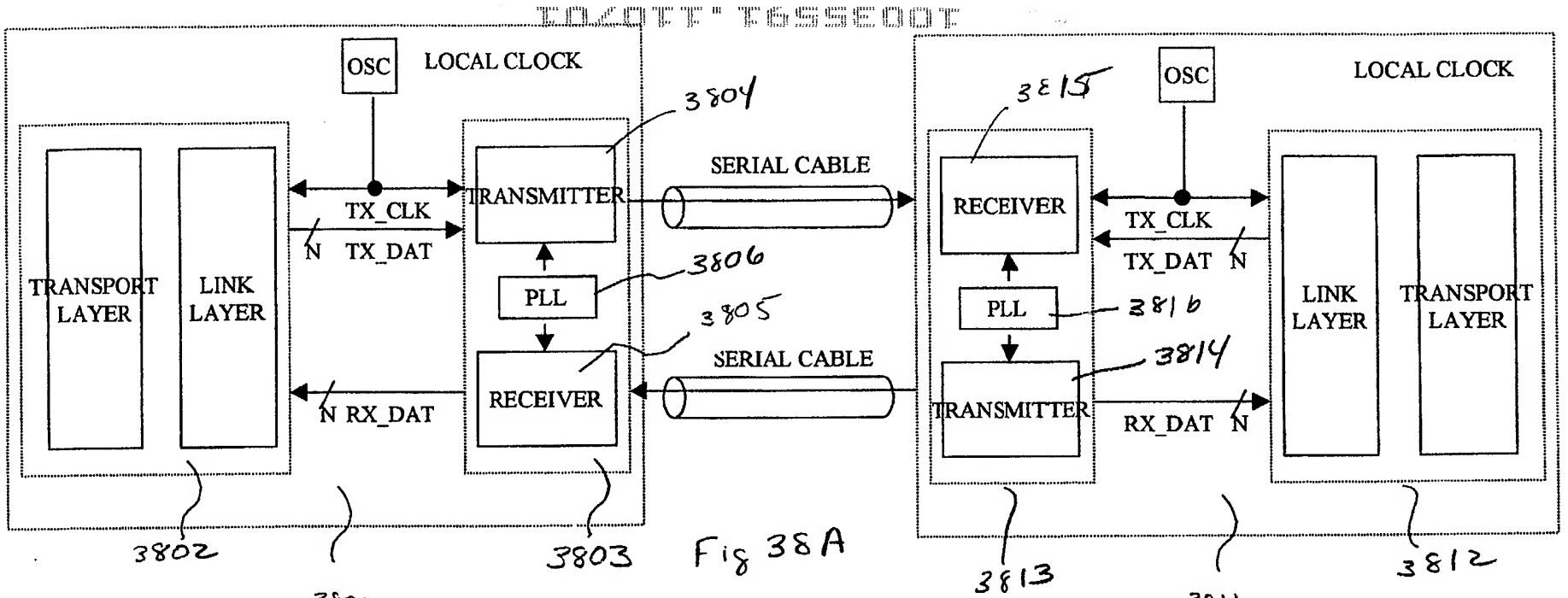



Fig 38A

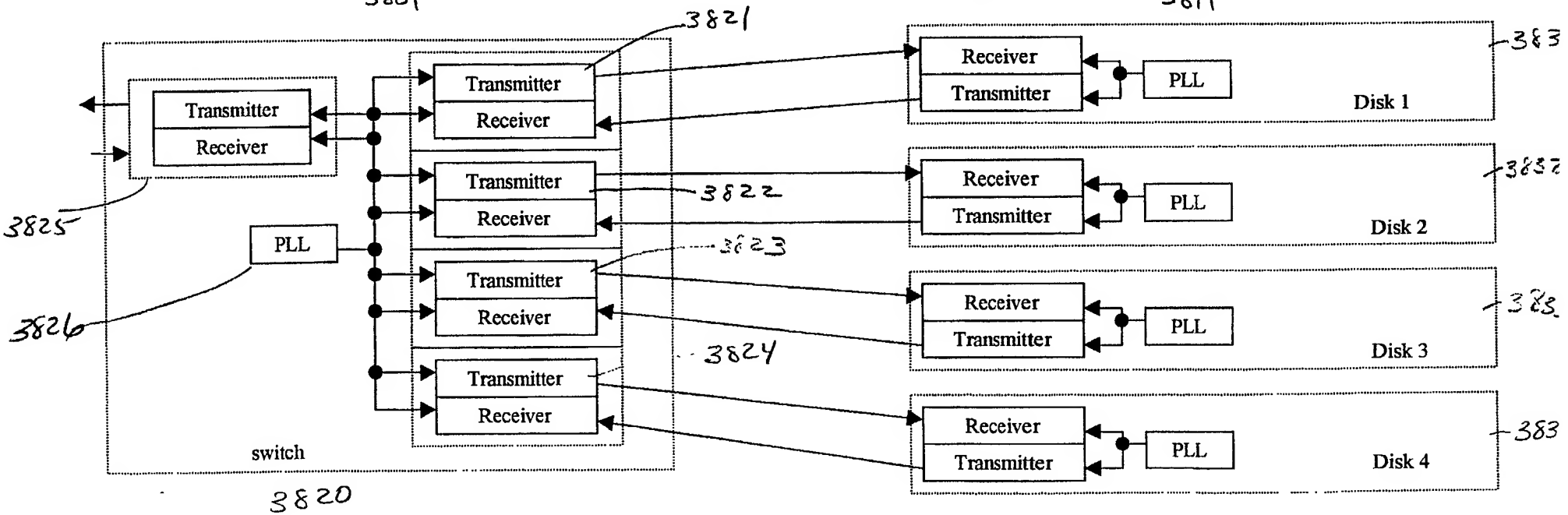



Fig 38B

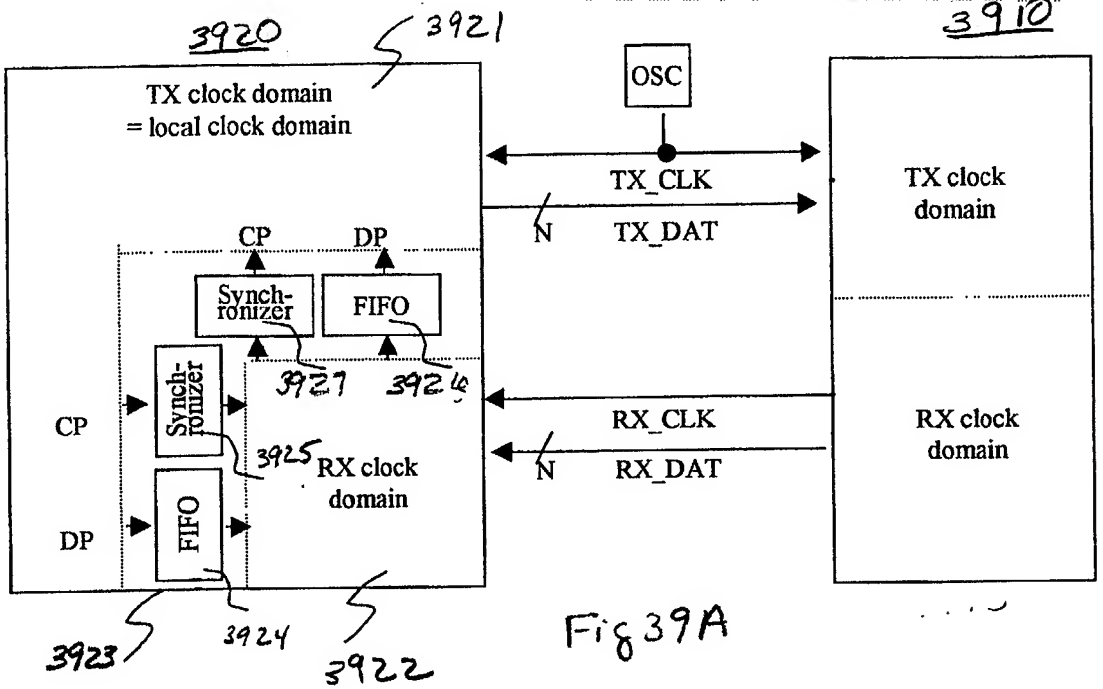



Fig 39A

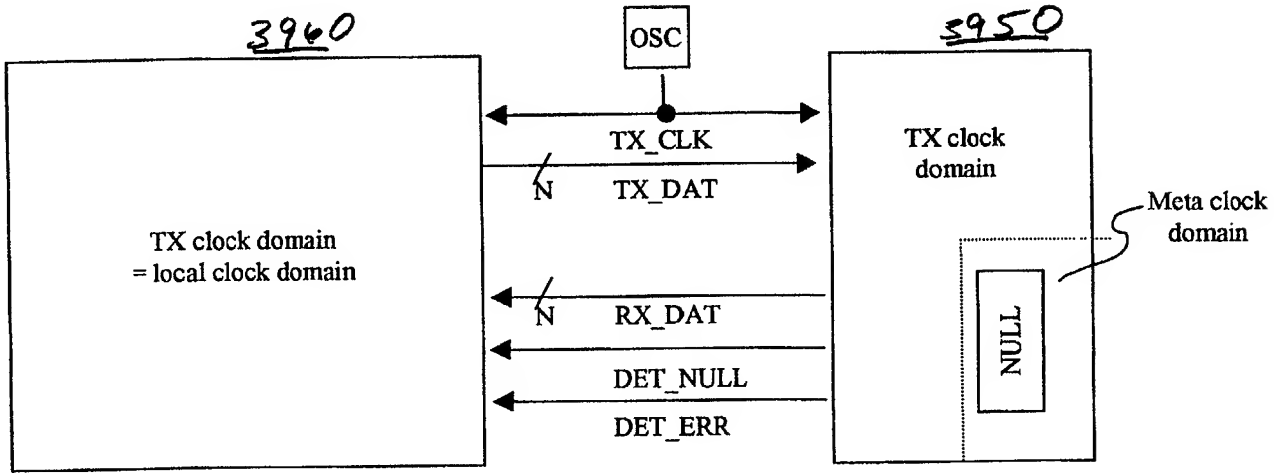



Fig 39B

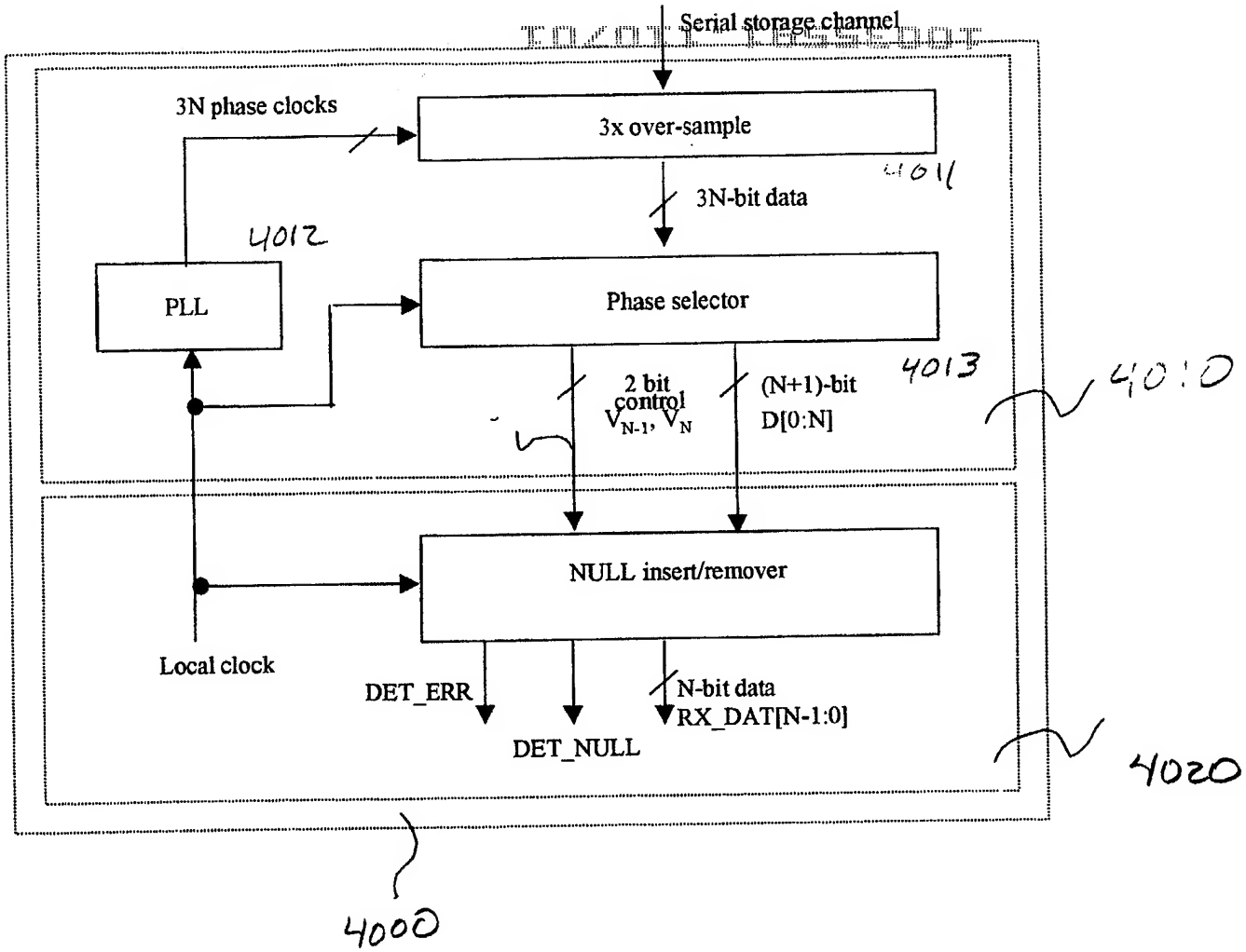

Serial storage channel
3N phase clocks
3x over-sample
4011
3N-bit data
4012
PLL
Phase selector
4013
2 bit control
$V_{N-1}$, $V_N$
(N+1)-bit
D[0:N]
4010
NULL insert/remover
Local clock
DET_ERR
DET_NULL
N-bit data
RX_DAT[N-1:0]
4020
4000

Fig 4D

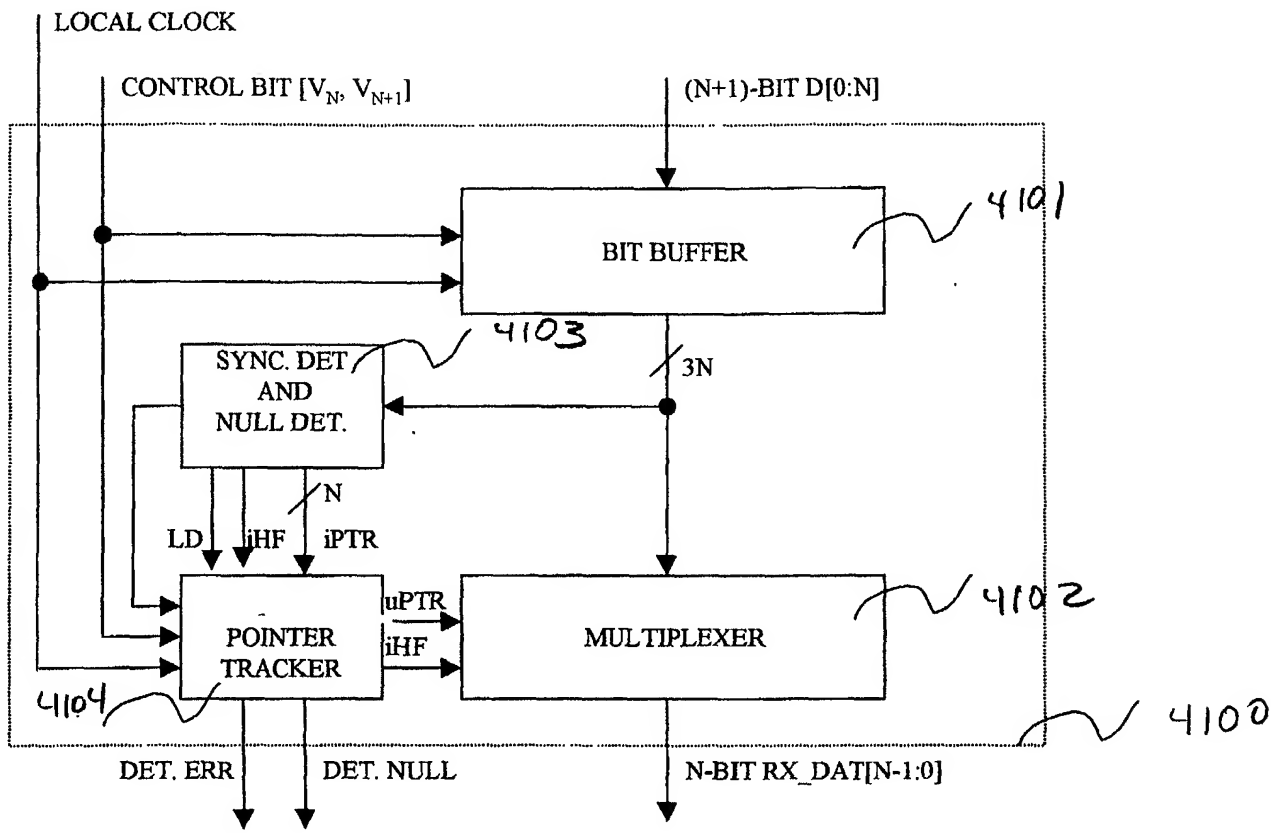



Fig 41

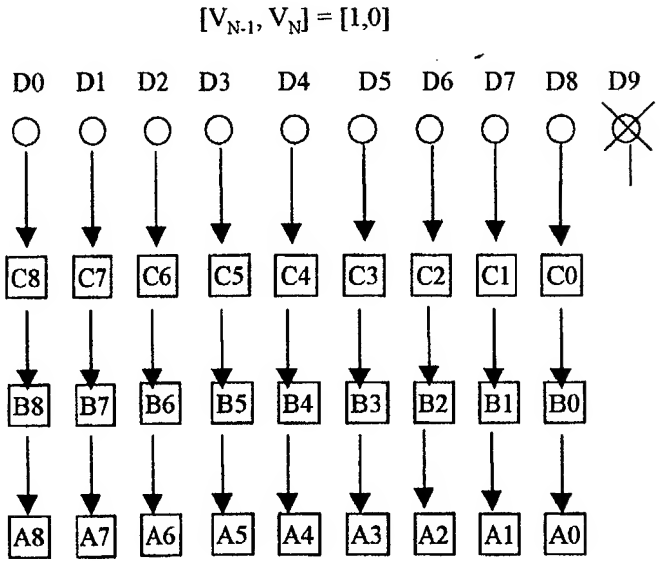

$[V_{N-1}, V_N] = [1,0]$
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9
C8 C7 C6 C5 C4 C3 C2 C1 C0
B8 B7 B6 B5 B4 B3 B2 B1 B0
A8 A7 A6 A5 A4 A3 A2 A1 A0

Fig 42A

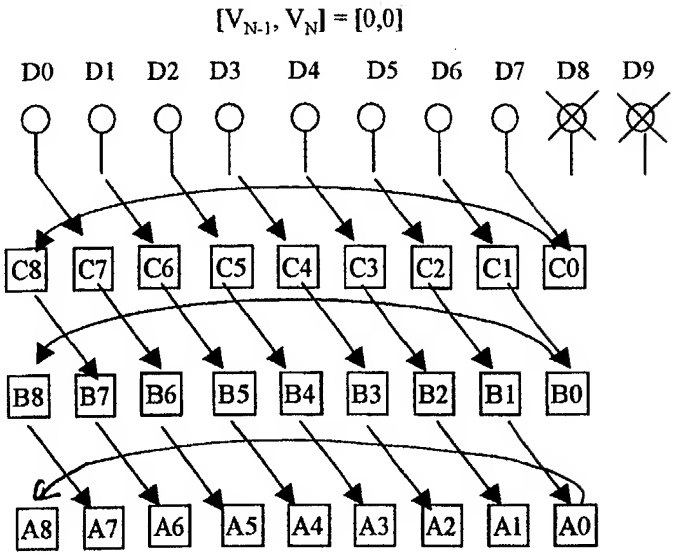



Fig 42B

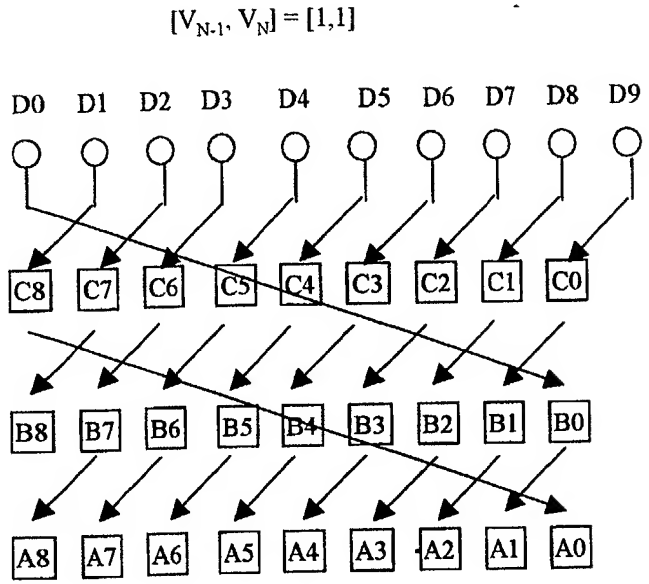

$[V_{N-1}, V_N] = [1,1]$
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9
C8 C7 C6 C5 C4 C3 C2 C1 C0
B8 B7 B6 B5 B4 B3 B2 B1 B0
A8 A7 A6 A5 A4 A3 A2 A1 A0

Fig 42C

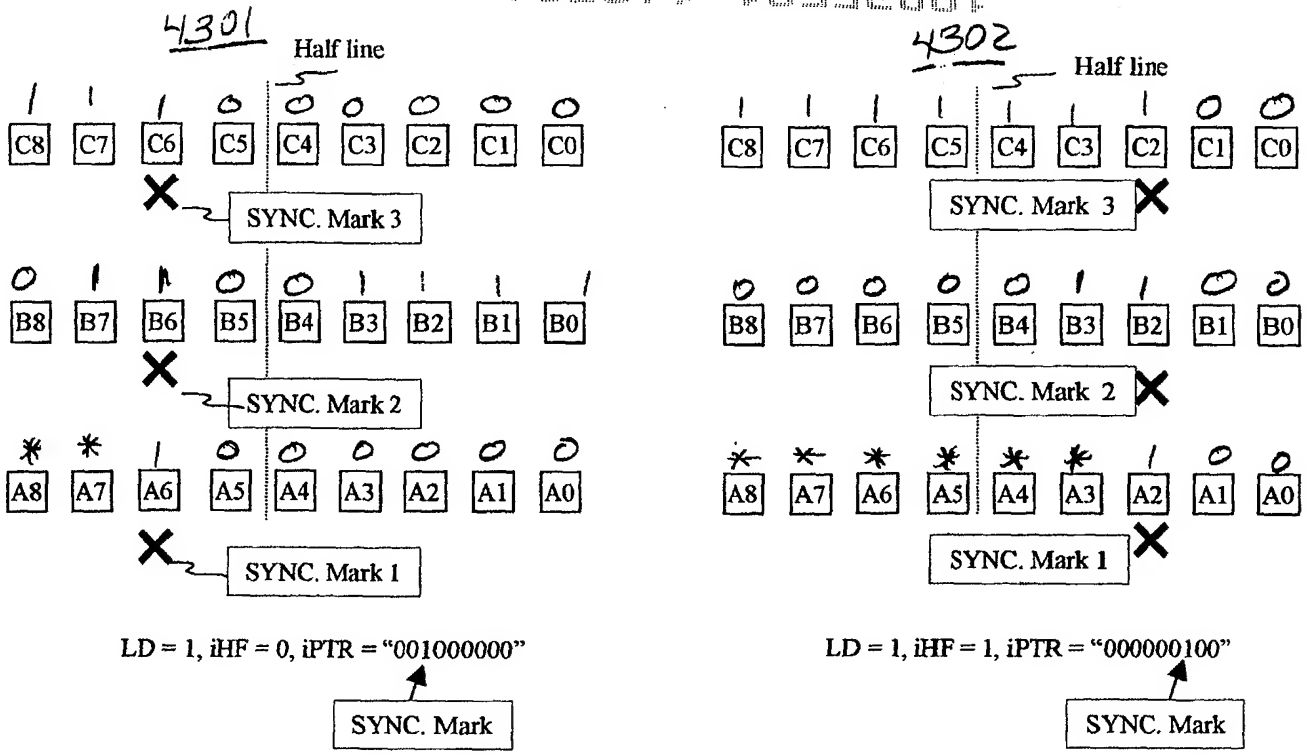
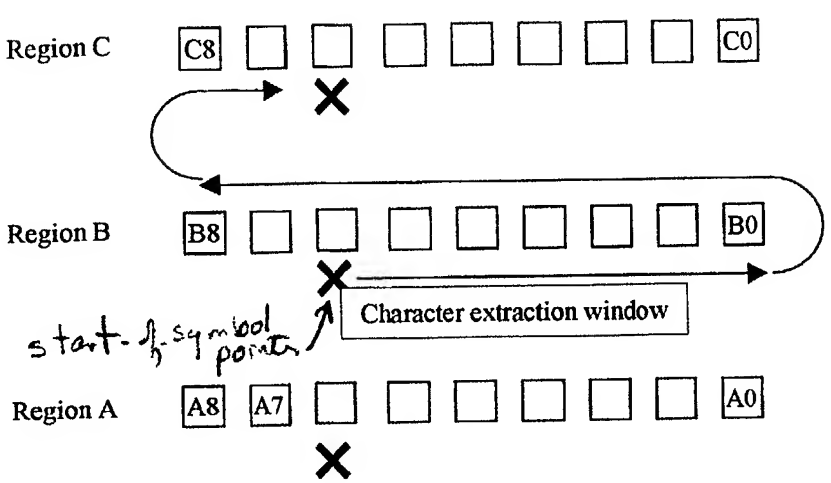
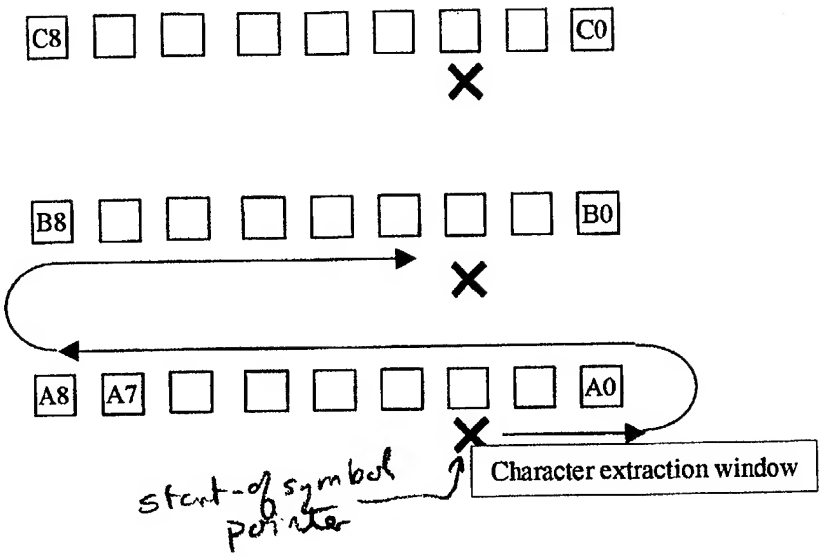



Fig. 43




LD = 1, iHF = 0, iPTR = "001000000"




LD = 1, iHF = 1, iPTR = "000000100"

Fig 44

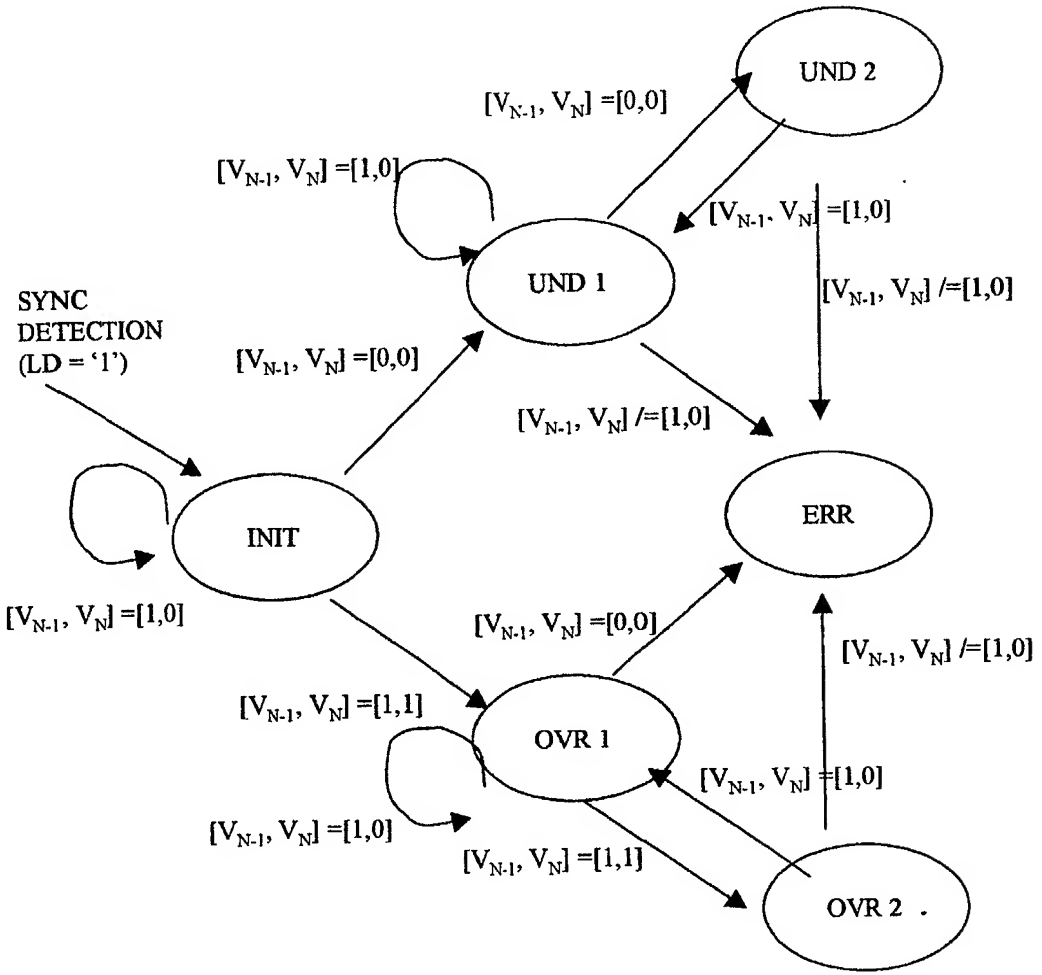

UND 2
$[V_{N-1}, V_N]$ =[0,0]
$[V_{N-1}, V_N]$ =[1,0]
$[V_{N-1}, V_N]$ =[1,0]
UND 1
$[V_{N-1}, V_N]$ /=[1,0]
SYNC
DETECTION
(LD = '1')
$[V_{N-1}, V_N]$ =[0,0]
$[V_{N-1}, V_N]$ /=[1,0]
ERR
INIT
$[V_{N-1}, V_N]$ =[1,0]
$[V_{N-1}, V_N]$ =[0,0]
$[V_{N-1}, V_N]$ /=[1,0]
$[V_{N-1}, V_N]$ =[1,1]
OVR 1
$[V_{N-1}, V_N]$ =[1,0]
$[V_{N-1}, V_N]$ =[1,0]
$[V_{N-1}, V_N]$ =[1,1]
OVR 2

Fig 45

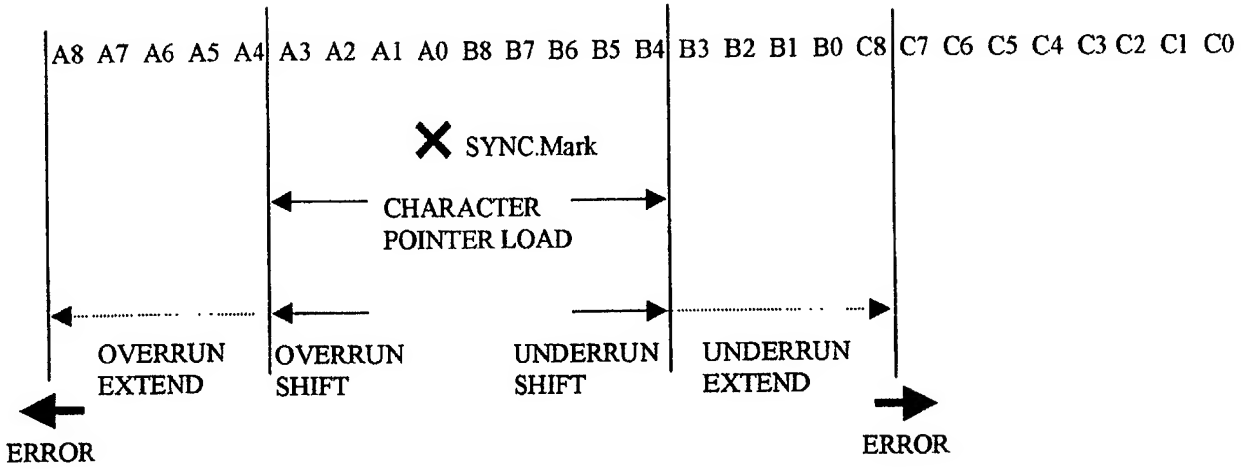

A8 A7 A6 A5 A4 A3 A2 A1 A0 B8 B7 B6 B5 B4 B3 B2 B1 B0 C8 C7 C6 C5 C4 C3 C2 C1 C0
SYNC.Mark
CHARACTER
POINTER LOAD
OVERRUN
EXTEND
OVERRUN
SHIFT
UNDERRUN
SHIFT
UNDERRUN
EXTEND
ERROR
ERROR

Fig 46

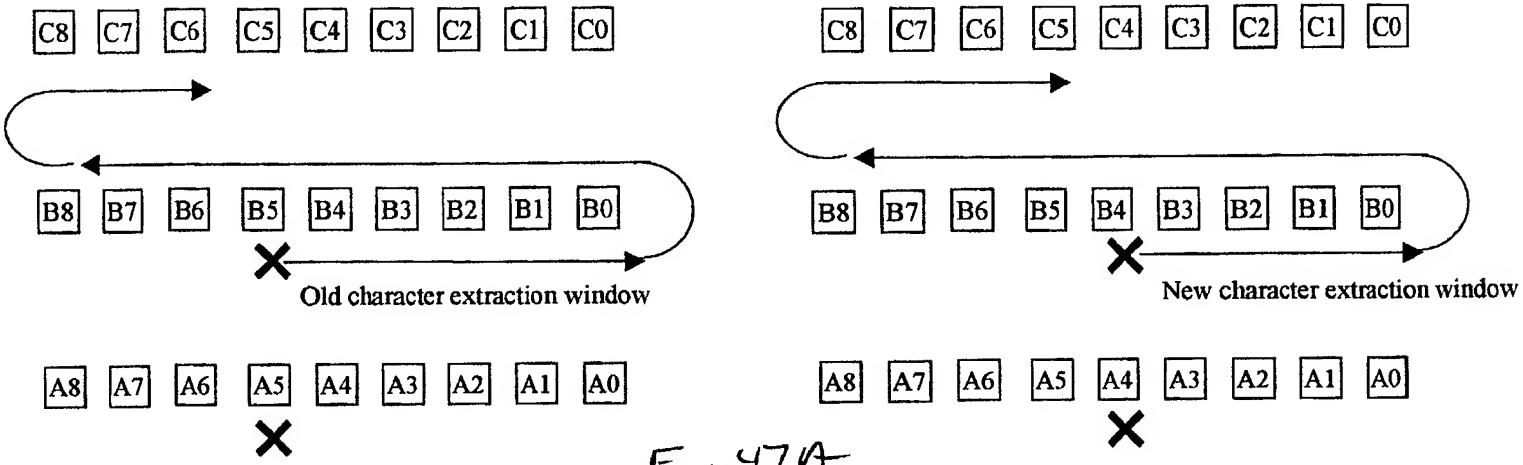



Fig 47A

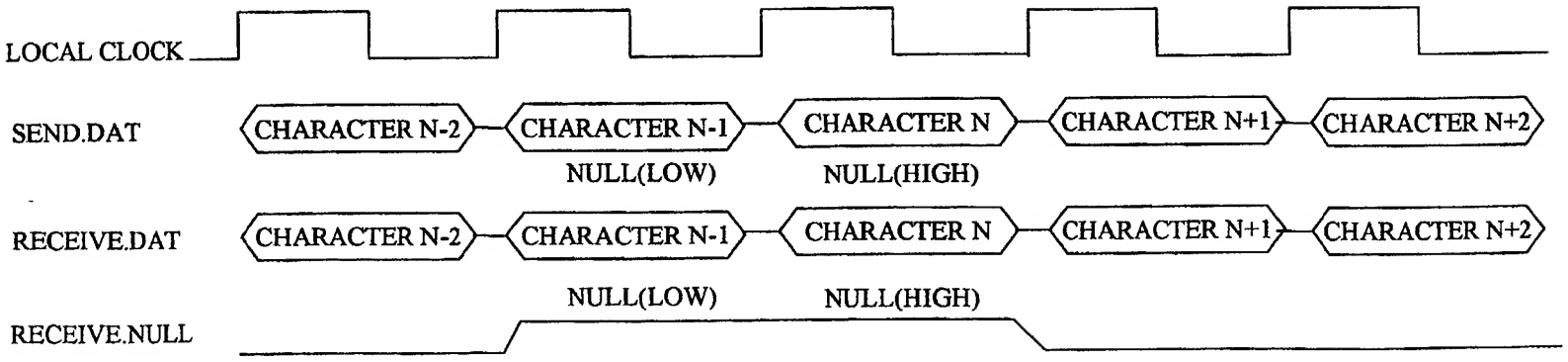



Fig 47B

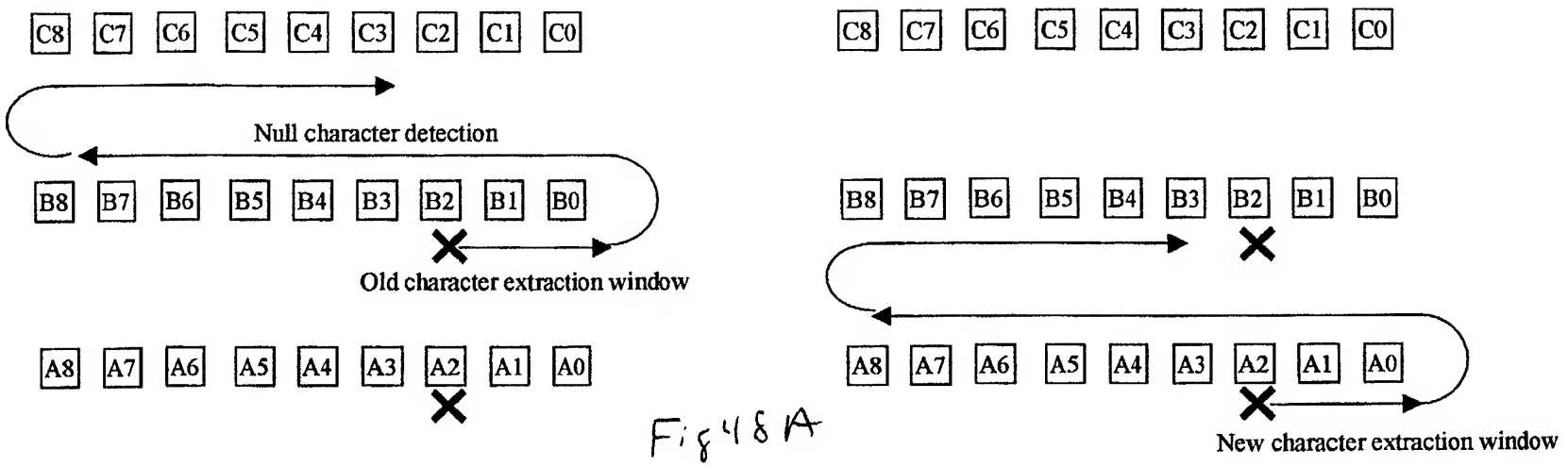



Fig 48A

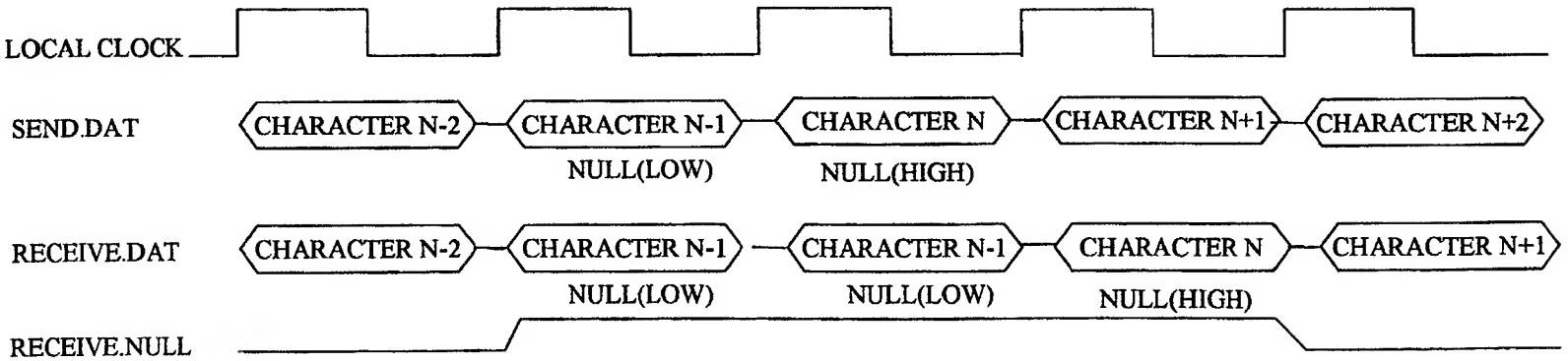



Fig 48B

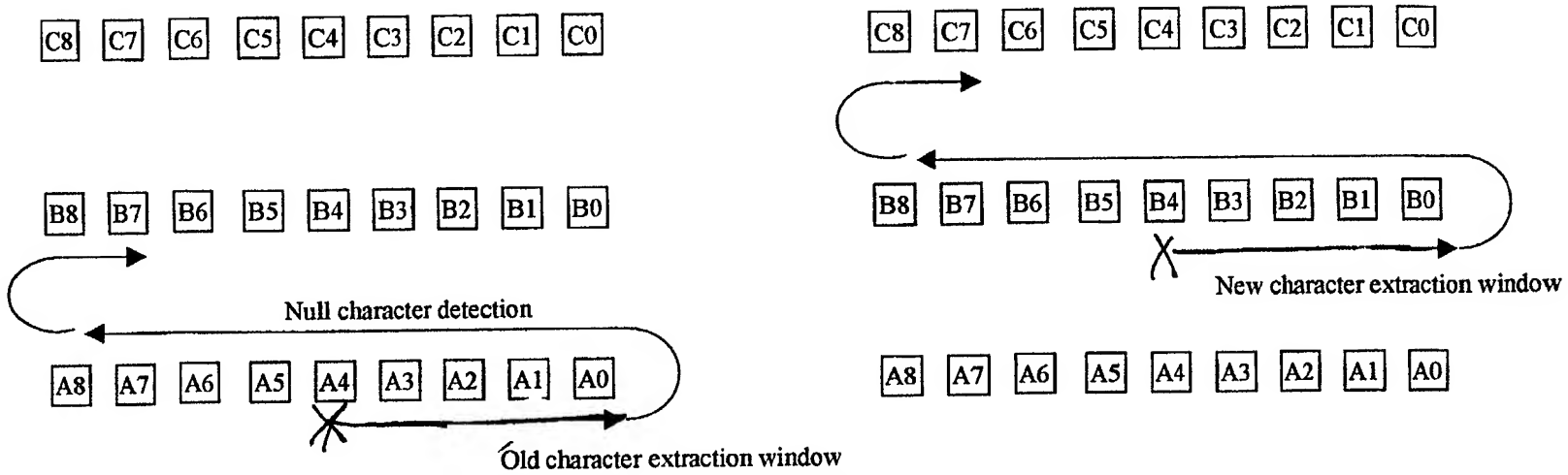



Fig. 49A

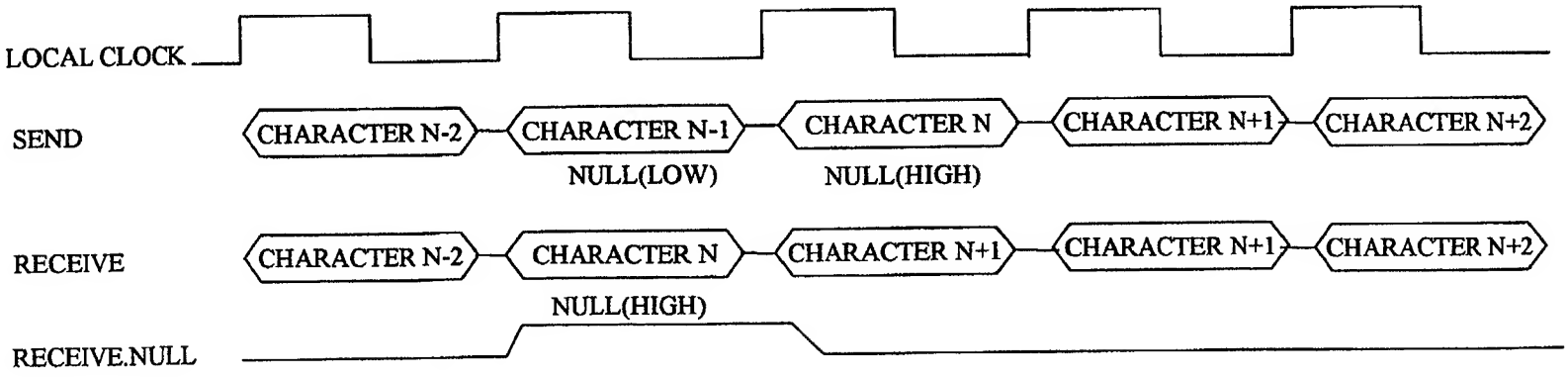



Fig 49B